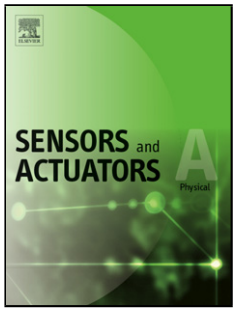

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A planar micro thermoelectric generator with high thermal resistance

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Abstract

This paper presents the modelling, design, fabrication and characterization of a planar micro thermoelectric generator (µTEG) which is able to convert waste heat into a few microwatts of electrical power. In order to get a better performance under a large variety of heat sources even if their thermal resistance is high, a planar µTEG with a large thermal resistance was designed and fabricated. It is built of two periodically etched silicon substrates that are respectively used as heat concentrator and heat evacuator, the whole embedding a multilayer membrane which includes a polysilicon-based thermopile with large thermoelement leg length. The thick air cavities etched in the substrates are effective in preventing the direct heat loss from concentrator to evacuator. 3D thermal simulations are carried out to improve the performance of the µTEG. A new definition of the "efficiency-factor" which involves the thermal input power instead of the temperature difference across the chip is suggested to evaluate the efficiency of this kind of µTEGs. The advantage of this new efficiency factor is that it takes the thermal resistance of the µTEG into consideration. With a thermal resistance of 78 K/W, the experimental results show that the µTEG can work under high temperature difference (up to 267K). With an optimised structure, ie 5 membranes and annealed polySi as TE main material, the maximum output power of our µTEG is 138 µW/cm^2 when the input power is 4 W/cm^2 and its corresponding new efficiency factor is 865 µm^2/W.

Keywords
Micro thermoelectric generator; Thermal resistance; Efficiency factor; Polysilicon; Figure of merit; micromachining

1. Introduction

With the need of decreasing the power consumption of more and more microelectronic systems, the power supply by energy harvesting in the proximate working environment is becoming more and more feasible. The micro thermoelectric generator (µTEG) which converts waste heat into electrical power is one of the many energy harvesting solutions [1]. Though the energy conversion efficiency of µTEGs is generally low [2], it is playing an important role in the field of energy harvesting mainly because of the abundance of sources of waste heat. Indeed, for instance natural ambient temperature cycle [3] or solar energy [4] can be used for thermoelectric power generation. Gathering heat dissipating from the human body through the skin surface by thermoelectric generators [5, 6] is an interesting way to develop wearable medical sensors.

There are two main categories of µTEGs related to the arrangement of the thermopile in a vertical or a planar architecture. Currently, most of the commercialised µTEGs are vertical structures (MPG-D751 by Micropelt [7], G2 modules by Tellurex [8], TGM by Kryotherm [9]), since they can usually deliver more output power than the planar µTEGs. This better performance of vertical µTEGs is often due to more powerful thermoelectric (TE) materials such as Bi_2Te_3 resulting in costly and non-environment friendly µTEGs, which limits their applications.
In this work, polysilicon layers are used as the thermoelectric material in the aim to develop a low-cost environment-friendly µTEG. Furthermore, the proposed topology permits the µTEG thermal resistance to reach quite high values: this is related to the planar structure that integrates polysilicon-based legs which have a low thickness and a great length. With such a high thermal resistance, the performance of the µTEG can be less weakened by the external thermal resistances which exist in real working conditions.
In the first part of this paper, will be given basic external-internal temperature analysis which permit to identify a new "efficiency-parameter" for qualifying better the impact of the external resistance. The design, modeling and fabrication of µTEGs will be presented in a second section. Their characterization once submitted to a calibrated heat flux will then be shown in a third section. Finally a

comparison between our µTEG and a reference µTEG reported in the literature will close this paper.

2. Basic considerations

In a vertical µTEG, the thermoelements X/Y of the thermopile are disposed normal to the flat surfaces of concentrator and evacuator, and most often X and Y are based on the same TE material in its two doped forms (n type and p type). In a planar µTEG, the thermopile is a flat line and concentrator and evacuator are geometrically structured in order to insure contacts alternatively with one junction over two. A simplified scheme of vertical and planar µTEGs is shown in Fig. 1.
When the concentrator is on contact with a heat source and the evacuator with a heat sink, respectively at temperatures T_{source} and T_{sink}, an effective temperature difference ΔT_e is created between two successive junctions of the thermopile.
As the thermopile is made of thermocouples connected in series, the open-circuit voltage generated at the two extremities of the thermopile is given by:

$$V_0 = n\alpha_{XY}\Delta T_e \quad \text{(V)} \quad (1)$$

Where n is the number of thermocouples, α_{XY} (V/K) is the relative Seebeck coefficient of the two thermoelectric materials X and Y. ΔT_e (K) is the effective temperature difference between each couple of junctions (Fig. 1).

To evaluate the ability of a thermocouple to efficiently produce thermoelectric power, a figure of merit Z [10, 11] is defined by way of thermodynamic considerations [12] taking into account all the thermal and electrical parameters of the two materials as:

$$Z_{XY} = \frac{\alpha_{XY}^2}{\left(\frac{\rho_X}{S_X}+\frac{\rho_Y}{S_Y}\right)(\lambda_X S_X + \lambda_Y S_Y)} \quad (K^{-1}) \quad (2)$$

Where λ_X, λ_Y (W/(m.K)) are the thermal conductivities and ρ_X, ρ_Y (Ω.m) electrical resistivities of the thermoelectric materials. S_x and S_y are the sections of the corresponding thermoelements.

For a µTEG constituted of n thermocouples, Z can be written as:

$$Z_{XY} = \frac{n^2\alpha_{XY}^2}{R_i K_e} \quad (K^{-1}) \quad (3)$$

Where R_i is the internal electrical resistance and K_e is the internal thermal conductance of the thermopile.

An apt optimisation of the architecture design of the µTEG is mandatory so as to enhance the µTEG ability to exploit most of the temperature difference between heat source and heat sink by adjusting thermoelements cross sections S_x and S_Y as:

$$\frac{S_X}{S_Y} = \sqrt{\frac{\lambda_Y \rho_X}{\lambda_X \rho_Y}} \quad (4)$$

And the optimal Z is:

$$(Z_{XY})_{opt} = \frac{\alpha_{XY}^2}{\left(\sqrt{\lambda_X \rho_X}+\sqrt{\lambda_Y \rho_Y}\right)^2} \quad (K^{-1}) \quad (5)$$

Many applications for energy harvesting [13, 14, 15] require µTEGs with low internal thermal conductance. In the next section it is shown that the output power delivered by the µTEG is maximum when the internal thermal conductance is equal to the environment-related conductance.
An easy way to achieve this criterion is to develop µTEGs with horizontal planar thermopile whose the thermal conductance K_e can be adjusted regardless of the electrical resistance R_i.

2.1 Simplified model

For both vertical and planar µTEGs, the thermal equivalent circuit diagram of a µTEG in working condition may be simplified as shown in Fig. 2, where r_{source}, $r_{\mu TEG}$, r_{sink} are the thermal resistances (K/W) of the heat source, of the µTEG and of the heat sink. The thermal contact resistance located between the heat source and the µTEG is noted r_c (K/W) and this one located between the heat sink and the µTEG is noted r_c'.

The thermal resistance of the whole µTEG ($r_{\mu TEG}$) can be divided into two parts: the effective thermal resistance of the thermopile $r_e = 1/K_e$ which leads to an effective temperature difference ΔT_e producing energy through Seebeck mechanism and a "parasitic" thermal resistance r_p which has no contribution on TE generation: $r_{\mu TEG} = r_e + r_p$. Obviously one has $\Delta T_e < \Delta T_c$, where ΔT_c is the temperature difference available between the concentrator and the evacuator.

For low Z_{XY} thermoelectric materials, for instance polysilicon, the effective output power and lateral heat losses are often negligible compared with the heat flows Φ_1 and Φ_2 (W), consequently Φ_1 and Φ_2 can be approximately considered equal as: $\Phi_1 \approx \Phi_2 \approx \Phi_e$. In this condition, the effective temperature difference between the hot/cold junctions can be expressed by [16]:

$$\Delta T_e = \frac{r_e}{r_e + r_{ex}} \Delta T_t \qquad \text{(K)} \qquad (6)$$

Where r_{ex} is the sum of all the external thermal resistances outside the thermopile: $r_{ex} = r_{source} + r_c + r_p + r_c' + r_{sink}$ and ΔT_t is the total temperature difference between the heat source and the heat sink (Fig. 2).

One has: $\Delta T_e < \Delta T_c < \Delta T_t$. So the maximum output power can be written:

$$P_{max} = \frac{V_0^2}{4R_i} = \frac{(n\alpha_{XY})^2}{4R_i} \left(\frac{r_e}{r_e + r_{ex}}\right)^2 \Delta T_t^2 \qquad \text{(W)} \qquad (7)$$

By introducing Eq.3, P_{max} is:

$$P_{max} = \frac{Z_{XY}}{4} \frac{r_e}{(r_e + r_{ex})^2} \Delta T_t^2 \qquad \text{(W)} \quad (8)$$

This output power will be maximized when the thermal adaptation criterion is realized; calculations yield the condition:

$$\frac{d(P_{max})}{d(r_e)} = 0 \qquad (9)$$

Which corresponds to the equality: $r_e = r_{ex}$ and P_{max} becomes:

$$(P_{max})_{opt} = \frac{Z_{XY}}{16} \frac{\Delta T_t^2}{r_{ex}} \qquad \text{(W)} \quad (10)$$

This equation (10) emphasizes the great interest to be able to adapt the thermal resistance of the µTEG (r_e) to its thermal environment that is possible with horizontal planar architecture.

2.2 Efficiency-factor

The maximum output power of a µTEG depends not only on thermoelectric material properties, but also on the topology of the device and on working conditions; that is why the classical figure of merit of the thermoelectric material Z is not enough to evaluate the performance of a given µTEG.
At present, a more complete coefficient is used in the literature: it's the so-called "efficiency-factor" (or device-power-factor) and is given by [17-19]:

$$F_e = \frac{P_{max}}{\Delta T_c^2 A_{\mu TEG}} \quad \text{(W/(K².m²))} \quad (11)$$

Where $A_{\mu TEG}$ is the area of the µTEG, P_{max} is the maximum output power and ΔT_C is the temperature difference between the external surfaces of concentrator and evacuator (Figs. 1 and 2). This power factor allows characterizing essentially the µTEG by taking into account its maximum output power available per unit of area and the temperature difference between its two faces.
However, in real working conditions, the thermal resistances outside the µTEG are difficult to be predicted and often not negligible, even bigger, compared with the thermal resistance of the µTEG. This often leads to a ΔT_C much lower than ΔT_t. For example, ΔT_C is 0.6% of ΔT_t in [17], 14.3% of ΔT_t in [18] and 3.8% of ΔT_t in [19]. The efficiency-factor defined by Eq.(11) is then not much representative of real efficiency of the device as the thermal resistance outside the µTEG is not negligible. So a high efficiency-factor cannot ensure a high output power if the µTEG thermal resistance is too small compared with the sum of the thermal resistances outside the µTEG.

That is the reason why we suggest a new definition of the efficiency-factor (F_e*) which takes into account the heat flow density φ_1 (W/m²) incoming in the µTEG instead of the temperature difference between the external surfaces of the µTEG. It will be defined by [20]:

$$F_e^* = \frac{P_{max}}{\varphi_1^2 A_{\mu TEG}} \approx \frac{P_{max}}{\varphi_e^2 A_{\mu TEG}} \quad \text{(m²/W)} \quad (12)$$

where φ_e (W/m²) is heat flow density going through the µTEG since $\varphi_1 \approx \varphi_2 \approx \varphi_e$:

$$\varphi_e = \frac{\Phi_e}{A_{\mu TEG}} = \frac{\Delta T_e}{A_{\mu TEG} r_e} \quad \text{(W/m²)} \quad (13)$$

With relations (6, 7), this leads to:

$$F_e^* = \frac{(n\alpha_{XY})^2}{4R_i K_e^2} A_{\mu TEG} \quad \text{(m²/W)} \quad (14)$$

By introducing Eq.3, we have:

$$F_e^* = \frac{Z_{XY}}{4} r_e A_{\mu TEG} \quad \text{(m²/W)} \quad (15)$$

By combining equations 10 and 15, one obtains:

$$(P_{max})_{opt} = F_e^* A_{\mu TEG} \frac{\Delta T_t^2}{4 r_{ex}^2} \quad \text{(W)} \quad (16)$$

This relation shows that if the thermal criterion r_e=r_{ex} is realized, the maximum power delivered by a µTEG can be easily computed knowing the parameters of the thermal environment (ΔT_t, r_{ex}).
Actually both the two power factors F_e and F_e^* are important for analysing the performance of the µTEG.

Assuming the area of the µTEG is equal to the area of its concentrator, the thermal resistance $r_{\mu TEG}$ of the µTEG is related to φ_e by the relation $\Delta T_C = r_{\mu TEG} A_{\mu TEG} \varphi_e$, using relations (11), (12) leads to the following relation between F_e and F_e^*:

$$F_e^* = F_e r_{\mu TEG}{}^2 A_{\mu TEG}{}^2 = F_e M^2 \qquad \text{(m²/W)} \qquad (17)$$

Where we identify M (K/(W/m²)) as a coefficient that we call the "intrinsic thermal resistive coefficient" of the µTEG.
In a first order approximation one can assume that the total thermal resistance outside the µTEG is inversely proportional to the area of the µTEG, the expression of this thermal resistance (r_{ex}) is given by:

$$r_{ex} = \frac{K}{A_{\mu TEG}} \qquad \text{(K/W)} \qquad (18)$$

Where K (expressed in K/(W/m²)) is named the "heat transfer coefficient".

When two different µTEGs (µTEG^A and µTEG^B) work under same working conditions (same ΔT_t and considering that this implies the same K), if the maximum output power per unit area of µTEG^A is always higher than that of µTEG^B regardless of the value of K, the performance of µTEG^A is 'better' than the performance of µTEG^B. This can be expressed by:

$$\frac{(n^A \alpha_{XY}{}^A)^2}{4R_i{}^A A_{\mu TEG}{}^A}\left(\frac{r_g{}^A}{r_{\mu TEG}{}^A + \frac{K}{A_{\mu TEG}{}^A}}\right)^2 \Delta T_t^2 \;>\; \frac{(n^B \alpha_{XY}{}^B)^2}{4R_i{}^B A_{\mu TEG}{}^B}\left(\frac{r_g{}^B}{r_{\mu TEG}{}^B + \frac{K}{A_{\mu TEG}{}^B}}\right)^2 \Delta T_t^2, \forall K \qquad (19)$$

It can be easily proved that the necessary and sufficient condition of relation (19) is that both the power factors (F_e and F_e^*) of µTEG^A are higher than those of µTEG^B, which can be expressed by:

$$(19) \Leftrightarrow F_e{}^A > F_e{}^B \;\; and \;\; F_e{}^{*A} > F_e{}^{*B} \qquad (20)$$

If one of the two µTEGs is not 'better' than the other, then it exists a heat transfer coefficient K_0 at which the performances of the two µTEGs are equal. In this case, based on equations (17) and (20), it can be proved that: if $M^A > M^B$, then $F_e{}^A < F_e{}^B$, $F_e{}^{*A} > F_e{}^{*B}$, and vice versa. This means that a µTEG with a higher 'intrinsic thermal resistive coefficient' (M) will deliver less output power per unit area when $K<K_0$ and more output power per unit area when $K>K_0$.
According to (17), the advantage of efficiency-factor F_e^* is that it takes the thermal resistance of the µTEG into consideration. It will be used in this work to show that the polysilicon-based planar µTEG realized here (with a high F_e^*) fits quite well the high external thermal resistance working conditions.

3. Realization of the µTEG

3.1 Design of the µTEG

The µTEG presented in this paper is derived from the same proprietary concept we developed for the fabrication of heat flux microsensors [21] and membrane-based IR microsensors [22]. We propose to design a µTEG composed of two parts: a periodically etched bottom silicon (Si) substrate with a multi-layer film (SiO_2/Si_xN_y/thermoelectric layer/polyimide) in which will be built a meandering path shaped thermopile (TE stripe periodically plated with a metal), and a top Si substrate which will concentrate the input thermal energy. This proposed topology is presented in Fig. 3.e.
The bottom Si evacuator is totally etched until the membrane at the place where are located thermopile hot junctions (see Fig. 3.f), while the thermopile cold junctions are placed above the evacuator pillars. The concentrator is aligned to the bottom substrate in such a way that its contacts with the thermopile are located at the hot junctions. The input heat flux is guided from the concentrator to the thermopile hot junctions through pillars (L_C wide and some 200µm tall), then it flows through the

membrane towards the pillars of the bottom evacuator which itself is placed on the heat sink. Hence a gradient of temperature ΔT_e is periodically created between each hot and cold couple of thermopile junctions, leading to the building of a total TE voltage available at the ends of the thermopile (Fig. 3.e). One can remark that the more thermally isolated are the hot and cold junctions, the higher is the temperature difference ΔT_e. That is why the thermopile will be built on a membrane embedded between top (200µm thick) and bottom (380µm thick) air cavities with long horizontal thermoelement legs (maximum length can be superior to 1mm).

3.2 3D thermal simulations

Given a certain amount of input power energy injected into the concentrator, it is relevant to calculate the temperature distribution in the µTEG and more precisely the temperature gradient ΔT_e as a function of the device parameters (number of membranes etc…), which ultimately will permit to determine the theoretical generated TE voltage. ΔT_e is related to the effective thermal resistance r_e (Fig.2) between two successive junctions and in this kind of µTEG, r_e depends on the thermal resistances of the thermopile (pSi/metal based), of its SiO_2/Si_xN_y support membrane, of the polyimide coating and of air cavities.
Considering the complexity of the architecture, 3D simulations operated with the COMSOL® software were carried out to investigate the temperature distribution within the µTEG [23].
For the modelling we set a fixed value for the area of the µTEG: 5.7×6mm^2 (which is a realistic value in order to fit to a layout of several µTEGs fabricated into Si wafers that are 3" diameter). In such circumstances when considering the modelling of µTEG devices with an increasing number of membranes N_m (typically 2 to 10), it is as considering thermocouples length that will be decreasing and their total number (n) increasing proportionally with N_m.

The thickness of the n-type polysilicon layer is 550nm, the carrier density is 2.6×10^{19}/cm^3 and the electrical resistivity is 0.0234$\Omega \cdot cm$. Its thermal conductivity is supposed to be 31W/(m.K) [24]. This value is not a critical parameter and a variation of +/- 20% has a minimal impact on the thermal resistance r_e because of the low thickness of the polysilicon layer. Indeed r_e essentially depends on the thermal resistances of the other layers arranged in parallel to the polysilicon layer which are lower.
A thermal contact resistance is induced by an air gap at the interface between the concentrator pillars and the polyimide top layer (Fig 3.b). This thermal resistance was modelled by the way of a 10 µm thick layer with a thermal conductivity adjusted to align experimental and theoretical results obtained from a set of µTEGs.
The obtained arbitrary value of 0.063W/(m.K) corresponds to an air gap depth of a few microns, which is consistent.
This first value for the thermal contact resistance was incorporated in the modelling and checked afterward that it is relevant for all the processed devices whatever their dimensions.
It can be noted that this contact resistance is very low compared with the total µTEG resistance due to the planar architecture.
The temperature distribution was modelled for different types of µTEGs. An example is given in Fig.4 for a 5 membranes µTEG with an incident power of 1W applied to the concentrator surface. Taking into account the concentrator area, the power density is 4W/cm² and the resulting temperature difference ΔT_e is found 78K.

In such condition the concentrator temperature is found to be 92K higher than the temperature of the evacuator. It can be noticed that there is no temperature gradient in the concentrator (red) or in the evacuator (blue) as a fact consistent with the very high thermal conductivity of Si substrates.

According to relation (7), the performance of various µTEGs can be simply evaluated by comparing the value of the quantity $\Delta T_e \times n$ or $\Delta T_e \times N_m$ (since n is proportional to N_m).
The temperature distributions, and $\Delta T_e \times N_m$, of a set of different µTEGs, with a number of membranes varying from 2 to 10, were computed versus the length of pillars L_c, while all the other parameters were kept fixed (which means the µTEGs have the same internal electrical resistance R_i). The obtained evolutions are drawn in Fig. 5, for an input power of 4W/cm^2. It is seen that the best theoretical µTEG performance is obtained with a 5 membranes configuration.
The knowledge of ΔT_e allows calculating the effective thermal resistance ($r_e = \Delta T_e / A_{\mu TEG} / \varphi_e$). On the other hand based on the computation of the temperature difference across the chip (ΔT_c, Fig.2), the thermal resistance of the µTEG ($r_{\mu TEG}$) can be deduced. Since the µTEG area is fixed, both thermal

resistances, r_e and $r_{\mu TEG}$, that are directly dependent on thermocouple (or membrane) length, will decrease with the number of membranes. This is illustrated Fig. 6. It can be noticed that the spacing between both curves represents the parasitic thermal resistance $r_p\,(N_m)$. This parasitic thermal resistance, rather small for a device with 2 membranes, starts to be superior to r_e when considering devices with more than 10 membranes.

The influence of the number of membranes N_m on the two efficiency-factors F_e and F_e^* defined in the previous section, can be deduced from the results of simulation considering relations (8), (11) and (15). Fig. 7 gives the trend obtained. Considering the new efficiency-factor F_e^*, a maximum value appears clearly for a µTEG designed with 5 membranes. This corresponds to a high effective thermal resistance r_e of 65K/W (Fig. 6). That shows the existence of an optimal configuration for 5-membranes devices.
On the opposite, the traditional efficiency-factor F_e increases continuously with the membrane number. Following our computations with N_m varying from 2 to 10, the maximum value is for a 10 membranes µTEG but its effective thermal resistance will be quite low (22 K/W). Increasing F_e through increasing N_m will decrease the thermal resistance of µTEG, which can limit the effective temperature difference ΔT_e in real working environment: this is clearly irrelevant for µTEG optimisation.
From the above described modelling results we decided to fabricate µTEGs with key configurations: ie. with 2, 5 and 10 membranes, which have respectively, the highest thermal resistance, the highest F_e^* and a higher F_e but with a parasitic resistance starting to be non negligible (~half r_e).

3.3. Fabrication

Three types of polysilicon (pSi) layers were used in this study for the fabrication of 3 families of planar µTEGs. The physical properties of these polysilicon layers are shown in Table 1. The PolySi No.1 is a standard polysilicon layer deposited on SiO_2/SiN covered Si (100) substrate by LPCVD (low pressure Chemical Vapor Deposition) and in situ doped with P (n-type).The layers PolySi No. 2 and PolySi No. 3 are grown with the same conditions as PolySi No.1. Then they have both been submitted to a rapid thermal annealing prior to any device processing in order to optimise their electrical and TE properties. In each case the electron concentration n_0 and the mobility μ are increased thanks to the thermal annealing; so the pSi resistivity can be strongly reduced ($\rho = 1/(n_0 e\mu)$), where $e = 1.6\times10^{-19}$C is the electron charge). However as the Seebeck coefficient is in parallel slightly reduced (because of the higher n_0, see Table 1) the power factor of polysilicon, α^2/ρ, is still superior in an annealed pSi than in a standard layer.

The realization of the µTEGs is based on a CMOS fabrication process starting from (100) oriented Silicon substrates (380 µm thick and 3-inch diameter) to fabricate the bottom evacuator part of the devices and the top heat concentrator.
The bottom part is realized on a first silicon wafer. The process is started by a thermal growth of a 0.8 µm oxide layer, then a LPCVD of 0.6 µm Si_xN_y is carried out which ultimately form the SiO_2/ Si_xN_y low-stressed film that will serve as the support layer of the thermopile [22] (Figs. 3.d and 8.a). The n-type pSi layer is then deposited by LPCVD (characteristics described earlier) (Fig. 8.b).
Then processing of several devices is carried out on each wafer by using a set of masks that integrates 2, 5 and 10 membranes based µTEGs and also other test modules as Van der Paw samples or TLM (transmission line model) patterns.

The dimension of all the µTEGs is $5.7\times6mm^2$. The meandering path shaped thermopiles are defined by classical lithography and are periodically covered by metallic plated thermoelements (Fig. 3) using lift-off techniques of a Ti/Al/Ni/Au (10nm/150nm/40nm/100nm) multilayer or a Al(240nm) layer for PolySi No. 2 wafer. A thermal annealing (450°C, 60min) process allows reducing the metal/polysilicon contact resistance to 7Ω. Because of the relative low electrical resistivity of the metallic thermoelements, the electrical resistance of the thermopile is mainly determined by the non-plated polysilicon part.
A 16µm thick layer of photosensitive polyimide HD-4110, with a low thermal conductivity of 0.2W/mK, is then deposited all over the µTEG surface except on the contact pad (Fig. 8.c). A high temperature annealing at 360°C allows obtaining fully controlled characteristics. This polyimide layer acts as passivation and electrical isolation layer between the thermopile and the heat concentrator.
The silicon substrate is then periodically plasma etched by ICP (Inductively Coupled Plasma) to release the membranes and to form the separating lines in between µTEGs and other modules (Fig. 8.d). A photography of a typical processed wafer after the membrane release is shown in Fig.9 where 44 µTEGs with 2, 5 or 10 membranes can be identified.

The 48 heat concentrators with (5.7×5.2mm^2) area are fabricated on a second 3" silicon wafer. A heating resistance (Ti/Au) dedicated to the generation of a calibrated heat-flow, is processed on one side (Fig. 3.c). Then, the back side is locally etched for a 200µm depth by ICP etching to form silicon pillars (2, 5 or 10 sets of pillar) (Fig. 8.e). The pillars situated at the centre of the concentrator will be aligned over on the middle of the membranes (Fig. 8.a). There are 4 supports at the corner of each concentrator that help preventing the central pillars to blow the membranes (Figs. 3.a and 3.b).

4. Experimental results

In order to mount the heat concentrator over the heat evacuator, an approximate alignment is realized by the home made system shown in Fig.10. In this first study we chose not to resort to any kind of glue.
Then to control the calibrating heat flow, the heating resistance on the top of the concentrator is connected to an electrical source by way of two "pogo pins". Taking into account the thermal environment of the µTEG (surrounded by polyester with a low thermal conductivity of 0.2W/mK), the heat flow density has been evaluated at approximately 80% of the delivered electrical power density by the way of a 2D model with Comsol®. The open-circuit voltage generated by the µTEG is measured with a precision voltmeter connected with two other pogo pins.

The output voltages of 8 µTEGs are measured for several heating conditions on the concentrator. The parameters of the 8 µTEGs are given in Table 2 together with one example of TE generation. The whole experimental results are shown in Fig. 11. It is seen that, as expected, the open-circuit voltage is proportional to the electrical input power generating the heat flow. With 1W of input power applied on the heat concentrator (3.32W/cm^2), the output voltage of µTEG^5 reached 9.68V. With an input power of 3W, one can achieve an output voltage in µTEG^1 as high as 20V, which corresponds to a 267K effective temperature difference between the hot/cold junctions (relation 1). This means that this kind of planar µTEGs can bear a very high temperature difference in working condition with a somewhat linear behaviour.

Using the Seebeck coefficients given in Table 1, the effective temperature difference (ΔT_e) can be easily deduced from each experimental output voltage and its evolution is plotted in Fig. 12. According to theoretical predictive result, ΔT_e should not be very sensitive to moderate changes in the TE layer (polysilicon) thermal conductivity because of its low thickness. This is indeed experimentally seen when comparing the behaviour of the 3 kinds of µTEG built with the 3 kinds of polySi: polySi which have been thermally annealed (No.2 and No.3) have a modified microstructure that, in one hand, results into a better thermopower, and on the other hand results into a higher thermal conductivity. But it seems that this change in thermal conductivity doesn't affect ΔT_e at all. Actually ΔT_e mainly depends on the length of the membranes. The highest ΔT_e is given by the 3 µTEGs designed with 2 membranes and the lowest ΔT_e is given by the 10 membranes µTEG.

In this study the best power factor is given by polysilicon No.3 (Table 1) and indeed it permitted to fabricate the more efficient µTEG. The µTEG^8 fabricated with this type of polysilicon has the highest output power (Fig. 13) because of the combination of an improved properties of this TE material associated with a 5-membranes topology and an optimised membrane length. The output power of µTEG^8 is 138µW/cm^2 when the electrical input power is 4W/cm^2.
In most of the literature, the thermal resistance of the µTEG is not indicated by the authors. This makes it difficult to compare the performances of µTEGs coming from different teams. Here we tentatively give a comparison with the work of T. Huesgen et al. [18]. In Table 3 are presented the characteristics of the µTEG^8 fabricated at IEMN compared to another planar µTEG developed in [18] which also uses polysilicon/metal as thermoelectric material.
Since the thermal resistance of our µTEG^8 is 50 times higher than the one given in [18], we calculated an efficiency-factor F_e^* approximately 10 times greater although the classical efficiency-factor F_e of our µTEG^8 is found 22 times lower. This shows that it is important to take both F_e and F_e^* into consideration during the evaluation of µTEGs. Moreover the thermal environment around the device proves to be critical considering the specifications for a given implementation.
To illustrate these results with a concrete case, let us consider these µTEGs glued on a heat sink, covered with blackbody layer and illuminated by the solar radiation about 1000 W/m². Under these conditions, the output power calculated by using F_e^* is 0.0297 µW for our µTEG^8 and only 0.0087 µW

for the other µTEG [18] though the area of our µTEG^8 is only 1/3 of that in [18]. So the temperature difference ΔT_C between the two sides of our µTEG^8 is 2.34K and only 0.15K for the other one.

In further work, the assemblage of the two parts of the µTEG (concentrator and evacuator) by a polyimide bonding technology, will offer a more accurate alignment and a more efficient heat flow. This technical operation will allow us to characterize the µTEG more precisely by using a characterization set-up already developed at the laboratory and used for heat flux-meter calibration [22].

5. Conclusion

This article reports on the conception and the realization of a new family of silicon planar thermoelectric microgenerators whose thermal conductance can be geometrically adjusted in the aim to produce a maximal electrical energy. Due to their low thermal conductance, a small incident heat flux density is enough to produce a significant output voltage (3V / (W/cm²)) easily usable by a DC-DC converter/controller.

These µTEGs were designed with respect of CMOS technology that avoid the utilization of polluting materials like Bi-Sb families. This eco-friendly characteristic coupled with the low thermal conductance allow their integration as power source in smart-dusts dedicated to be disseminated in the nature, using latent heat induced by natural change of state of water: dew, froze, rain evaporation/icing.

A new definition of the efficiency-factor (F_e^*) was defined and justified. It involves the incident heat flux density instead of the temperature difference ΔT_c between the two sides of the chip used for the classical efficiency-factor F_e.

Indeed, the measurement of ΔT_c requires the insertion of temperature sensors on each side of the microgenerator. The induced thermal parasitic resistances are very difficult to evaluate and should be taken into account, especially when the thermal conductance of the µTEG is high.

Contrary, the new definition of the efficiency-factor F_e^* is easy to be accurately computed because the incident heat flux (Φ_1) is very few perturbed by contact resistances and can be easily produced by infrared radiation or with a small planar heating resistance thermally insulated on one side.

Moreover, by using F_e^* when the parameters of the thermal environment are known it is very easy to compute and maximize the electrical power delivered by the µTEG whose the thermal resistance verify the adaptation criterion.

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List of figure captions

Fig. 1. Schematic of cross-sectional views of a vertical µTEG (a) and a planar µTEG (b) connected to a load resistance.

Fig. 2. Simplified thermal equivalent circuit diagram of a vertical or planar µTEG in working condition.

Fig. 3. Photos of parts of the µTEG: (a), (b): the concentrator, (c): the heating resistance dedicated to the generation of a calibrated heat-flow. SEM images of the polysilicon layer supported by the SiO2/ SixNy low-stressed film (d). Schematic **(**e) of the planar 3-membranes µTEG and simplified representation of the heat flow path (f) on the cross section along the A-A' line.

Fig. 4. Temperature distribution simulated with 3D COMSOL® for a 5-membranes µTEG. One notices there is no temperature gradient in the concentrator or in the evacuator.

Fig. 5. Evolution of $\Delta T_e \times N_m$ versus L_c as a function of the membranes number of the µTEG for an input power density of 4 W/cm².

Fig. 6. Total and effective thermal resistances of the µTEGs versus the membrane number (in the simulations, L_c is kept to 200µm).

Fig. 7. Evolution of two efficiency-factors with number of membranes (F_e and F_e* are normalized by $F_{e(2membranes)}$ and $F_e{}^*{}_{(2membranes)}$, respectively).

Fig. 8. Flow chart of the µTEG fabrication process;

Fig. 9. Top side (a) and back side (b) photos of a 3'' wafer after releasing the membranes. The 48 heat concentrators with 5.7×5.2mm² areas are processed on a second silicon wafer.

Fig. 10. The alignment and measurement system.

Fig. 11. Open-circuit voltage versus electrical input power density.

Fig. 12. Effective temperature difference ΔT_e versus electrical input power density.

Fig. 13. Maximum output power versus electrical input power density.

List of tables

	PolySi No.1	PolySi No.2	PolySi No.3
Thickness(nm)	550	600	730
Carrier density (/cm^3) n_0	2.6×10^{19}	4.5×10^{19}	7.5×10^{19}
Resistivity ρ ($\Omega\cdot cm$)	0.0234	0.007	0.0038
Seebeck coefficient (μV/K) at 25°C	260	225	178
Mobility μ (cm^{2}V^{-1}s^{-1})	10.2	20	22
Power factor α^2/ρ (μW/cm/K^2)	2.9	7.2	8.4

Highligths

Planar thermoelectric microgenerators were designed with respect to CMOS technology.

A new efficiency-factor involving heat flux and thermal resistance is introduced.

Efficiency is optimisable by the way of the microgenerator thermal resistance.

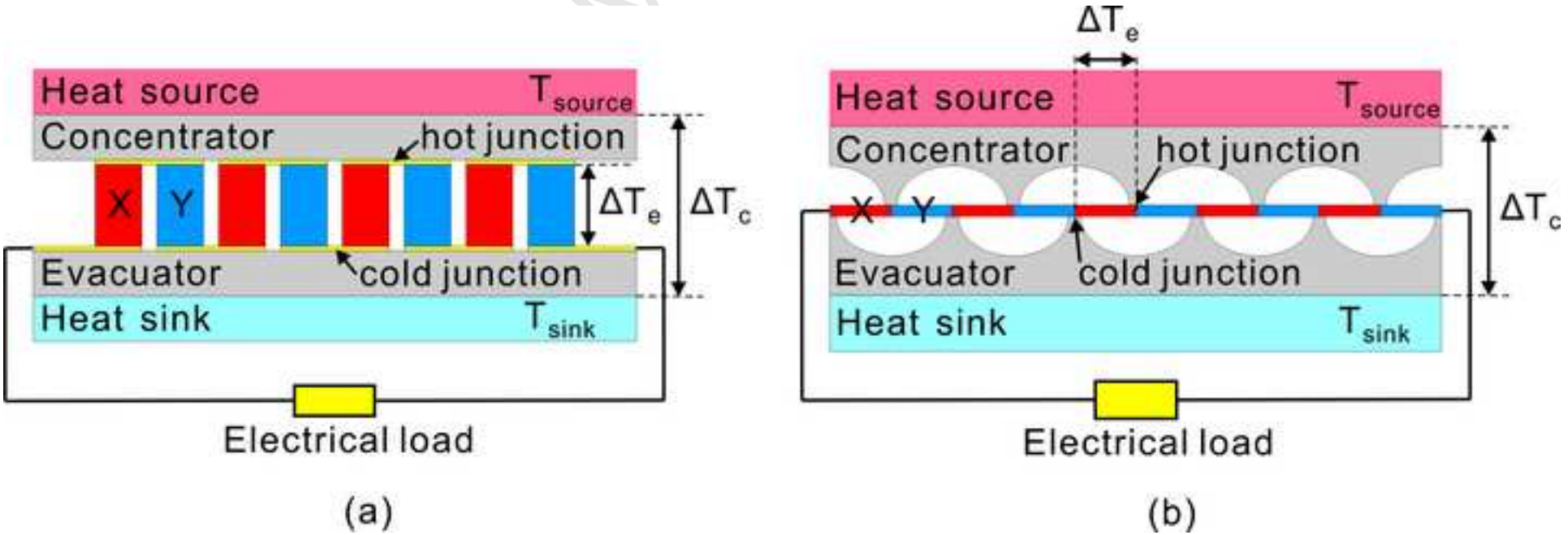
The microgenerator thermal resistance is adjustable via its geometrical dimensions.

For 4W/cm^2 input power, the output power is 138µW/cm^2 and efficiency factor 865µm^2/W.

	μTEG[1]	μTEG[2]	μTEG[3]	μTEG[4]	μTEG[5]	μTEG[6]	μTEG[7]	μTEG[8]
Polysilicon type	No.1	No.1	No.1	No.2	No.2	No.2	No.3	No.3
Number of membranes	2	5	10	2	5	5	2	5
Polysilicon width (μm)	50	70	50	50	50	70	50	70
Number of thermocouples	288	560	1440	288	720	560	288	560
Membrane length (μm)	2300	800	300	2300	800	800	2300	800
Contact length L_c (μm)	1150	400	150	1150	400	400	1150	400
Electrical resistance R_i (M Ω)	2.94	1.73	2.94	1.22	1.06	0.56	0.38	0.234
Seebeck Output Voltage for 1W injection (V)	6.33	8.22	6.85	5.78	9,68	7.38	5	5.54
Max output power for 1W injection (μW/cm²)	9.9	28.4	11.6	19.9	64.2	70.71	47.9	95.3

	μTEG[8] IEMN	μTEG by T.Huesgen et al. [18]
Area of μTEG	5.73mm×6mm	10mm×10mm
Total thermal resistance of the μTEG $r_{\mu TEG}$ (K/W)	78	1.555
$F_e = \frac{P_{out}}{\Delta T_c^{\,2} A_{\mu TEG}}$ (μW/(cm^{2}K^2))	0.0163	0.363
$F_e^* = \frac{P_{out}}{\varphi_e^{\,2} A_{\mu TEG}}$ (μm^2/W))	865	87

Figure 1



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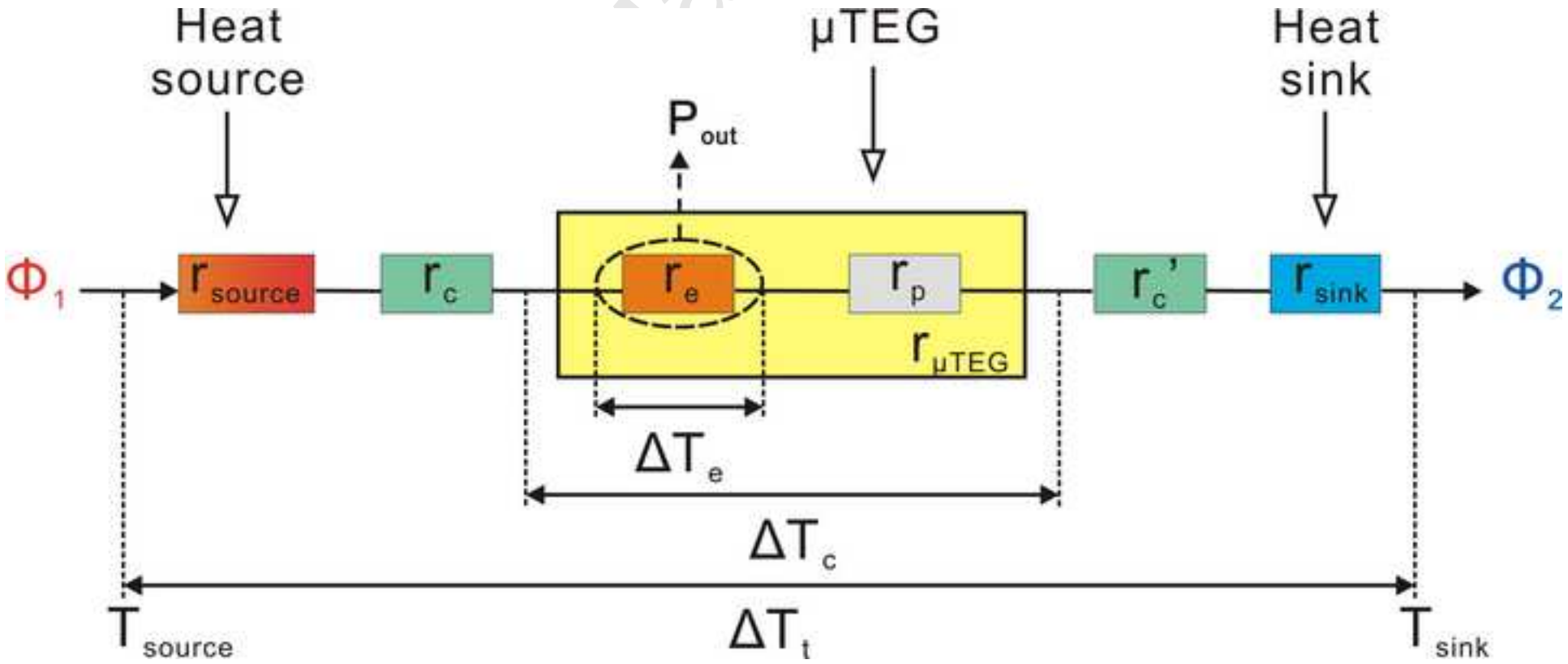

Heat source
μTEG
Heat sink
P out
Φ1
r source
r c
r e
r p
r c'
r sink
Φ2
r μTEG
ΔT e
ΔT c
ΔT t
T source
T sink

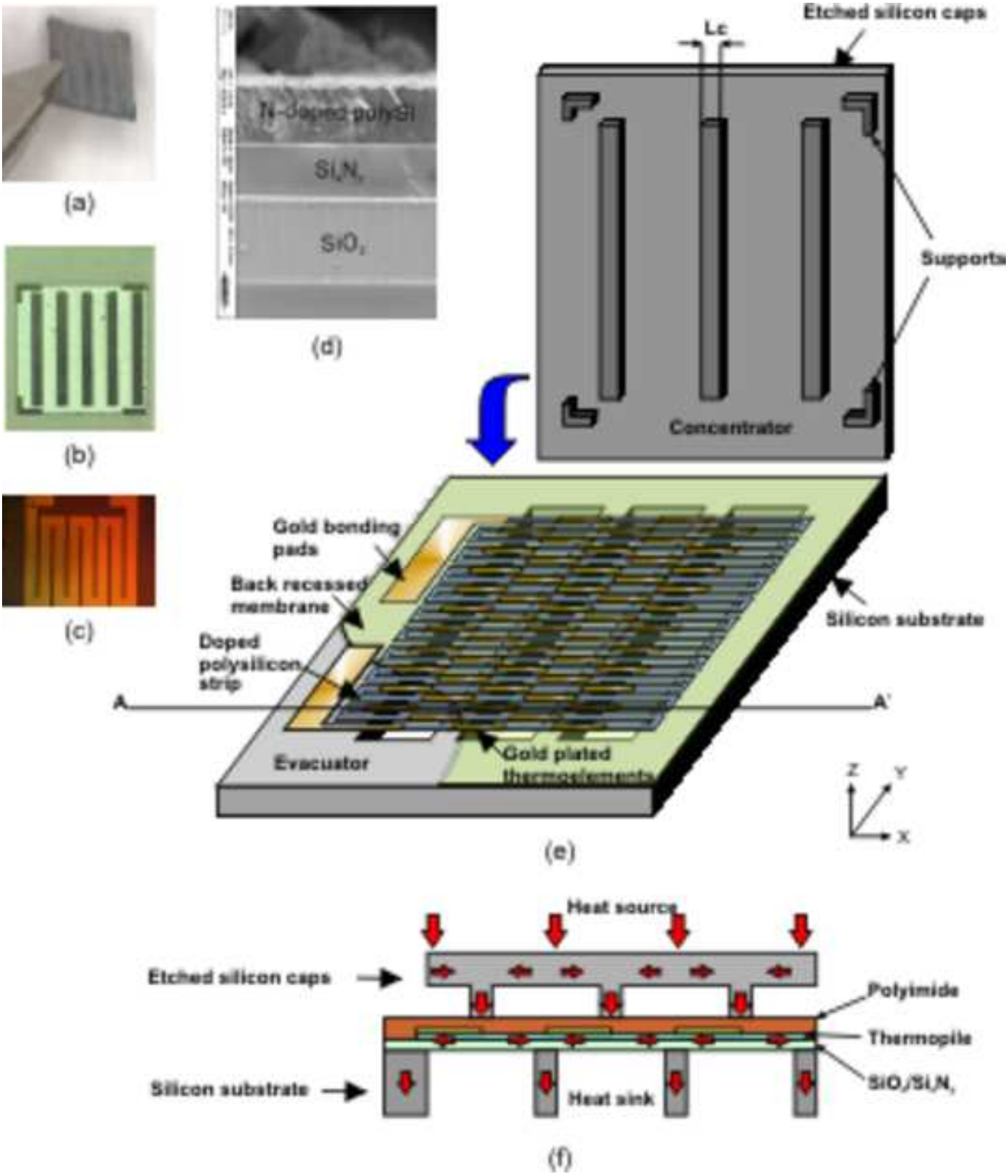


Figure4

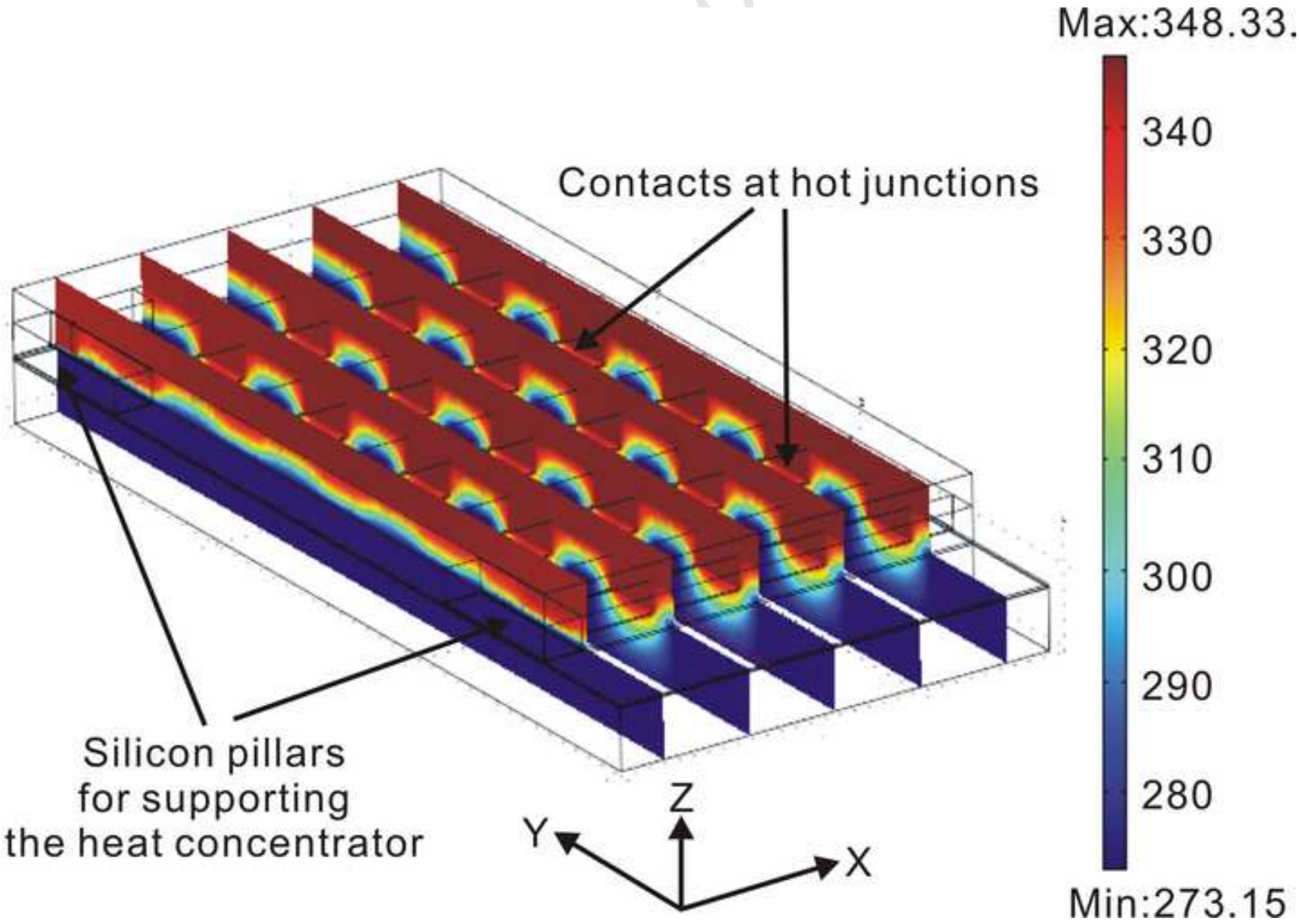

Max:348.33.
340
330
320
310
300
290
280
Min:273.15
Contacts at hot junctions
Silicon pillars
for supporting
the heat concentrator
Z
Y
X

Figure5

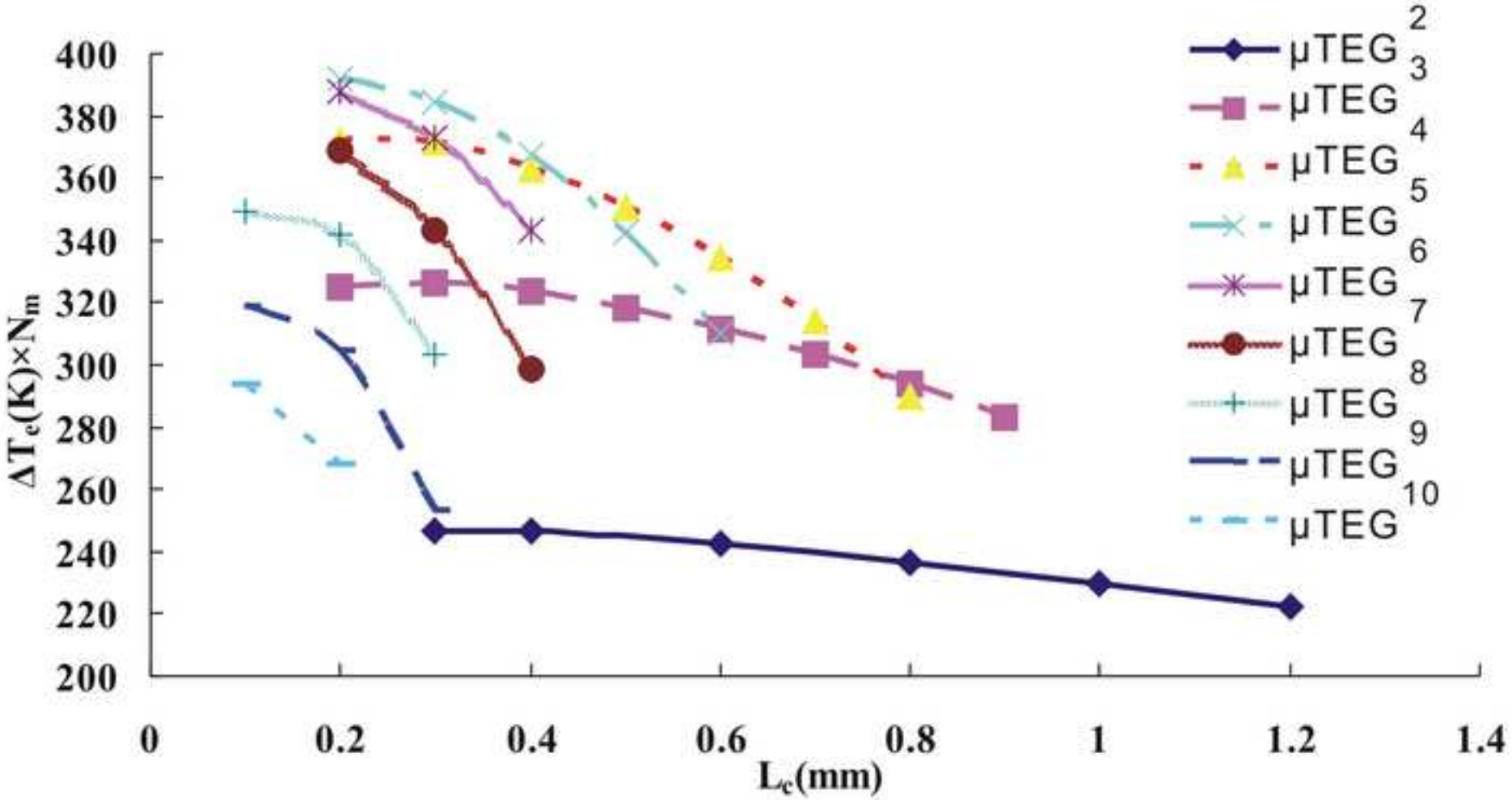

400
380
360
340
320
300
280
260
240
220
200
ΔTe(K)×Nm
0
0.2
0.4
0.6
0.8
1
1.2
1.4
Lc(mm)
2 μTEG
3 μTEG
4 μTEG
5 μTEG
6 μTEG
7 μTEG
8 μTEG
9 μTEG
10 μTEG

Figure6

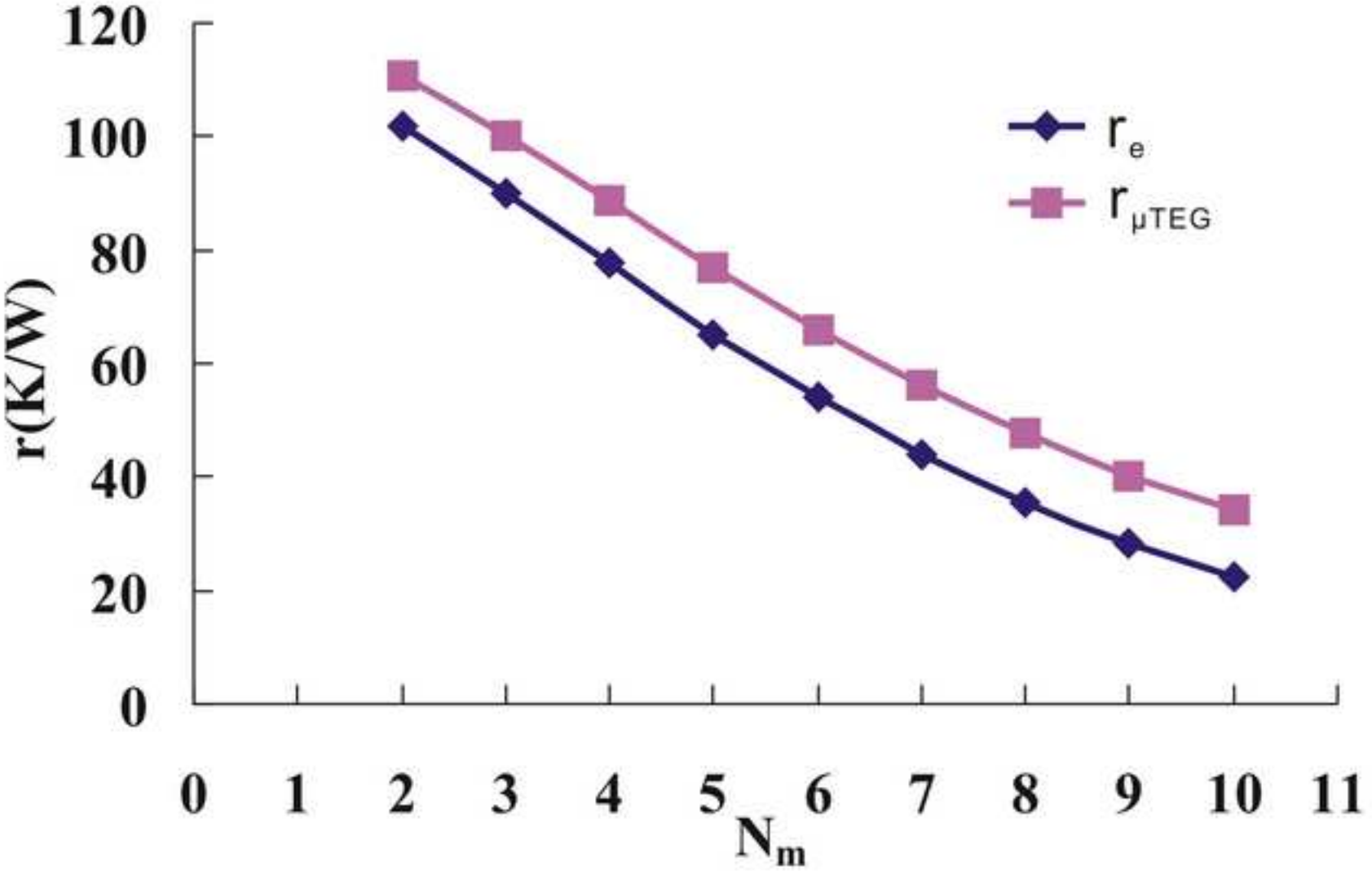
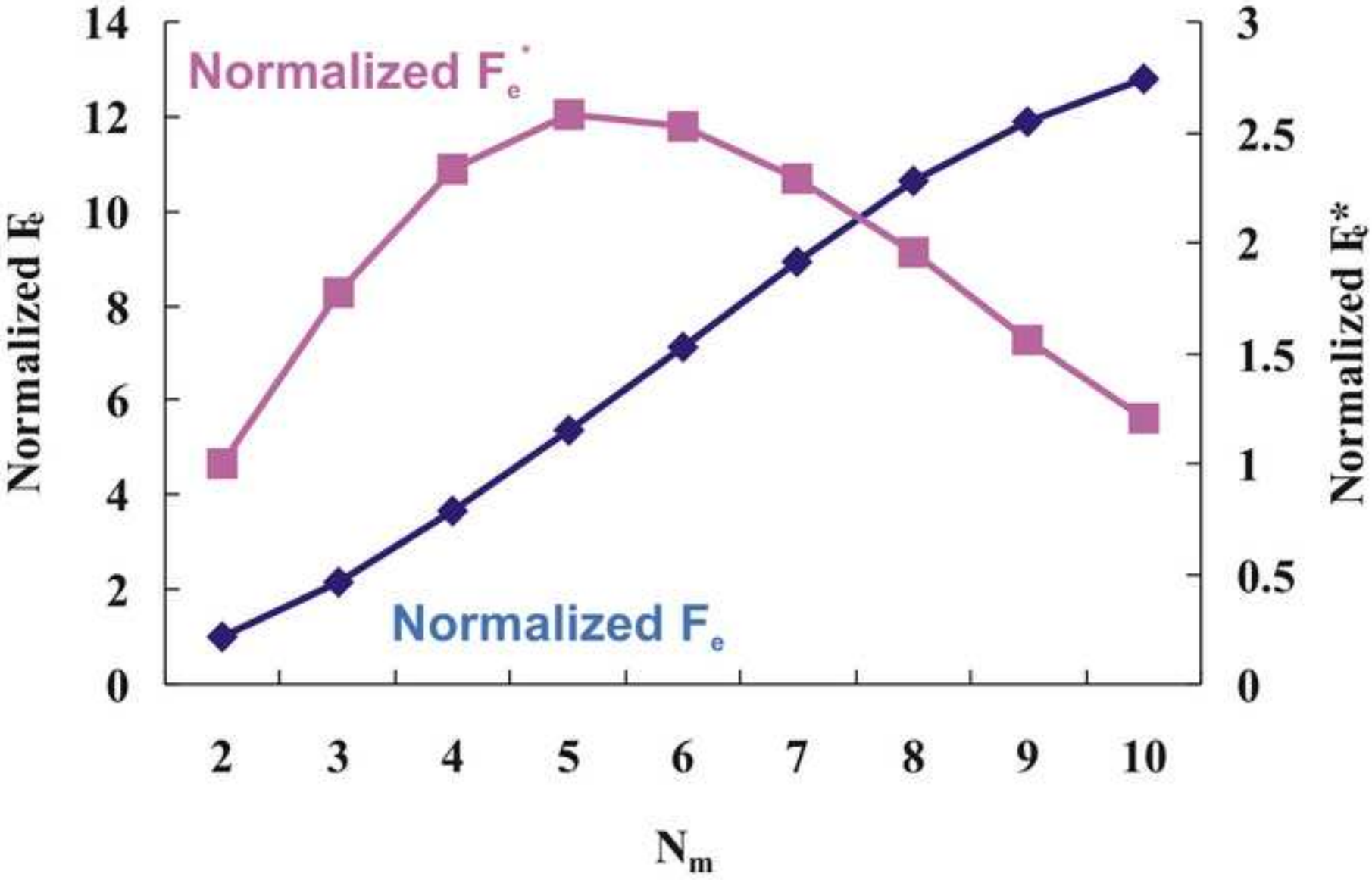


Figure7


Normalized F_e*
Normalized F_e
Normalized F_e
Normalized F_e*
N_m
0
2
4
6
8
10
12
14
0
0.5
1
1.5
2
2.5
3
2
3
4
5
6
7
8
9
10

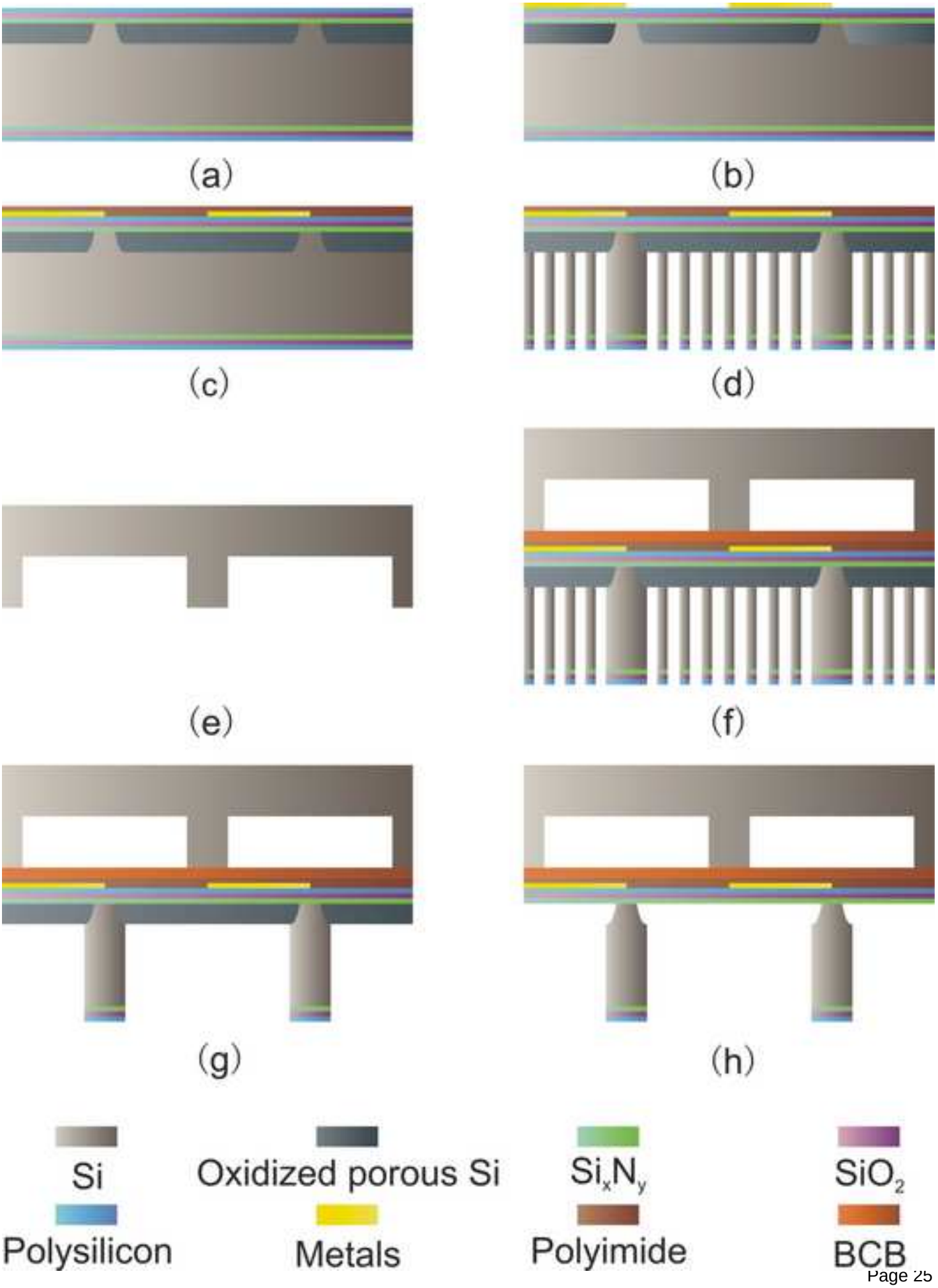
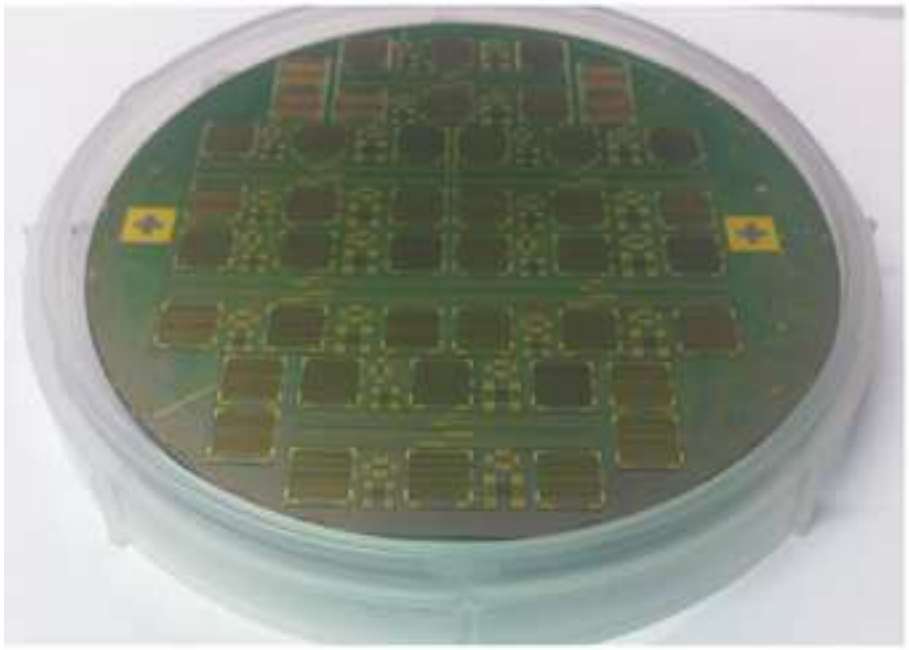
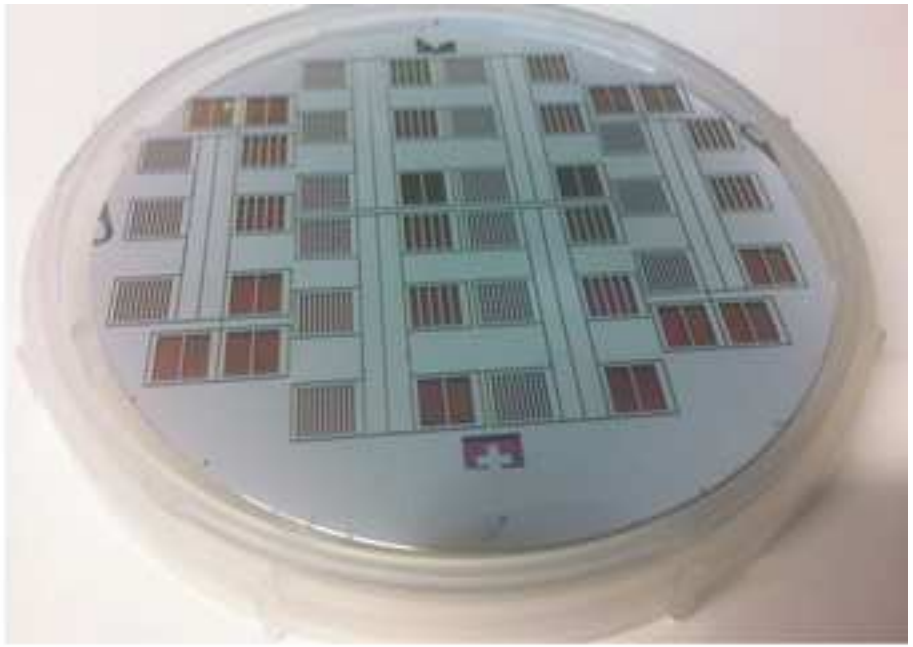


Figure9



(a)



(b)

Figure 10

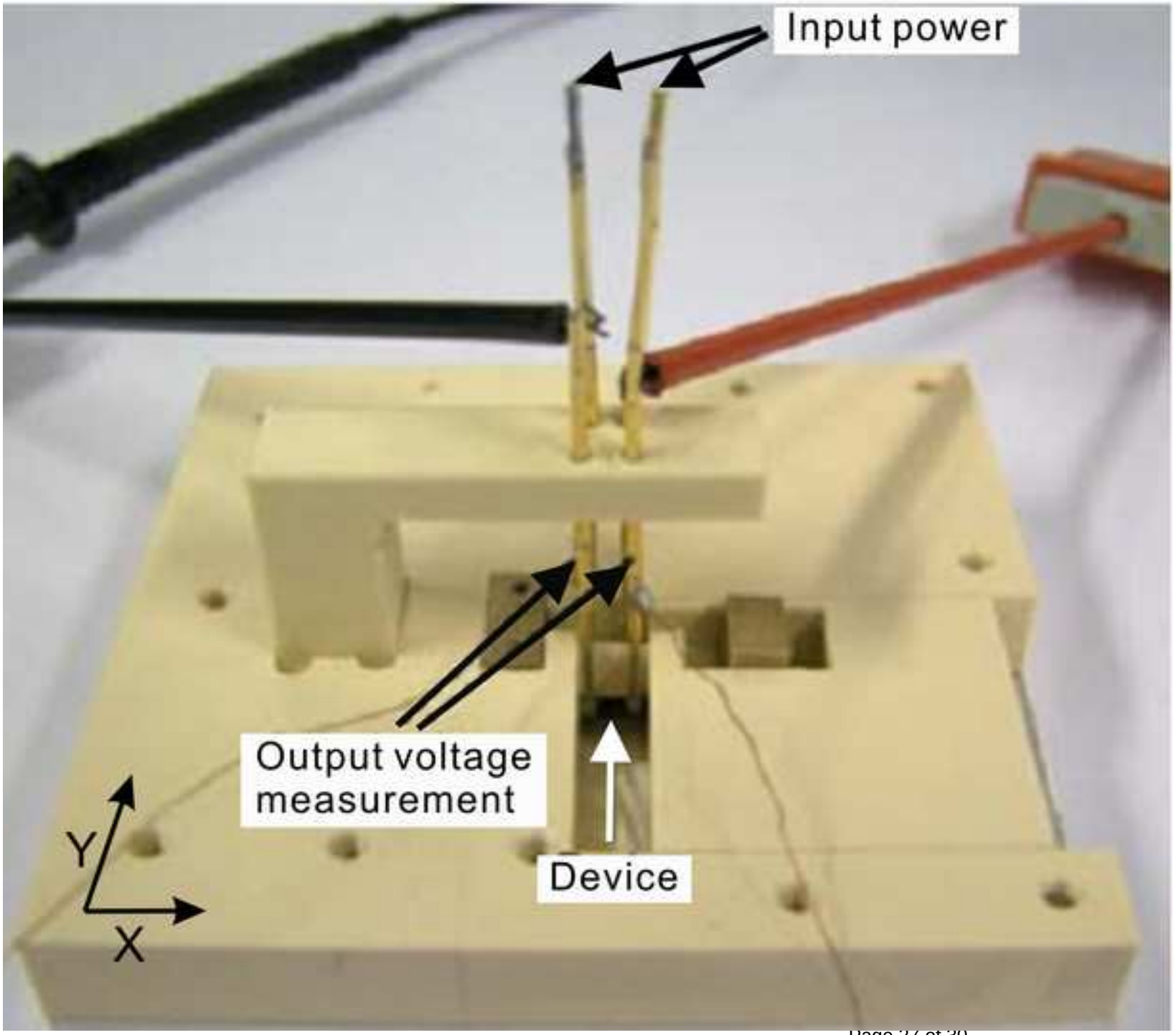


Figure11

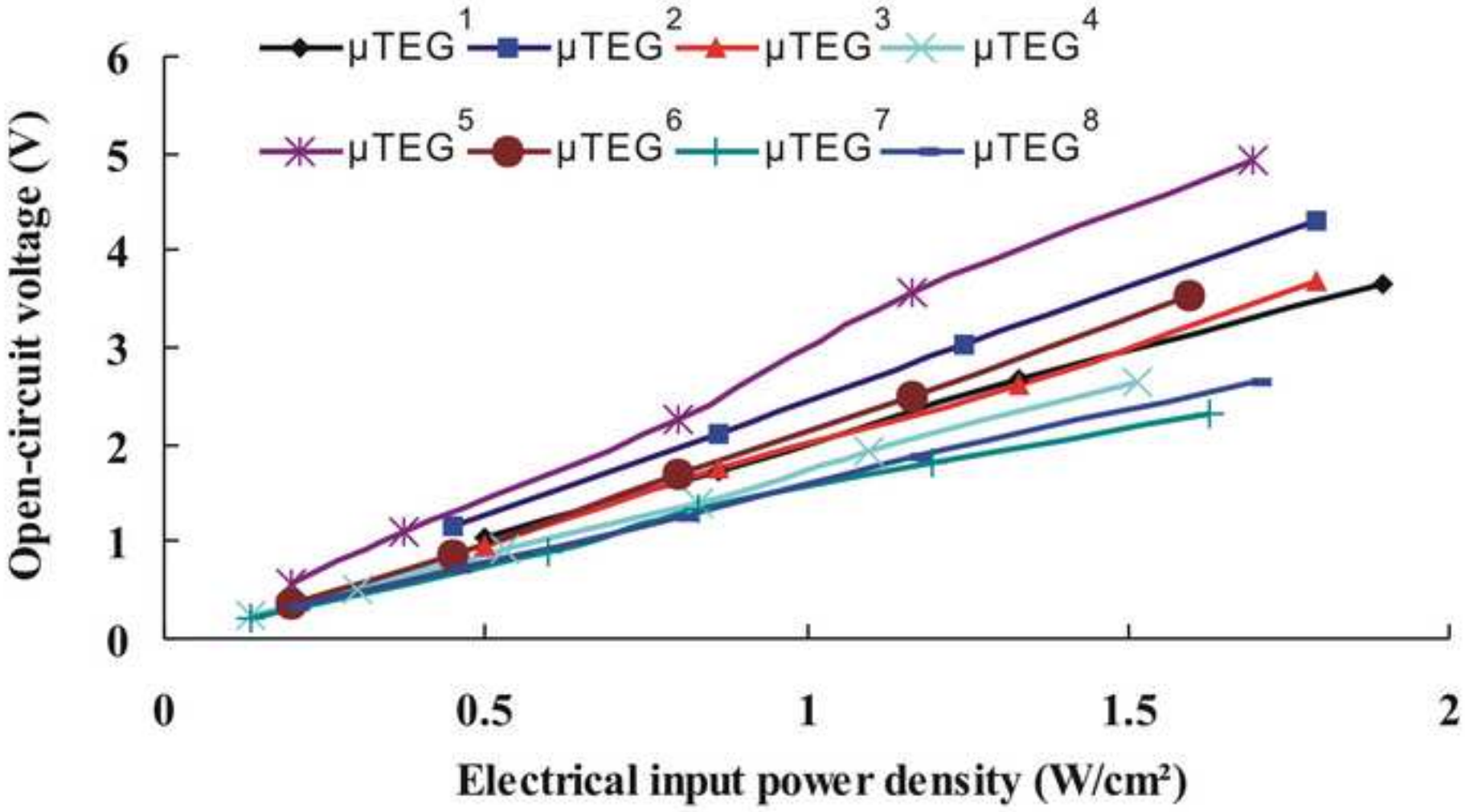

μTEG 1
μTEG 2
μTEG 3
μTEG 4
μTEG 5
μTEG 6
μTEG 7
μTEG 8
Open-circuit voltage (V)
0
1
2
3
4
5
6
0
0.5
1
1.5
2
Electrical input power density (W/cm²)

Figure12

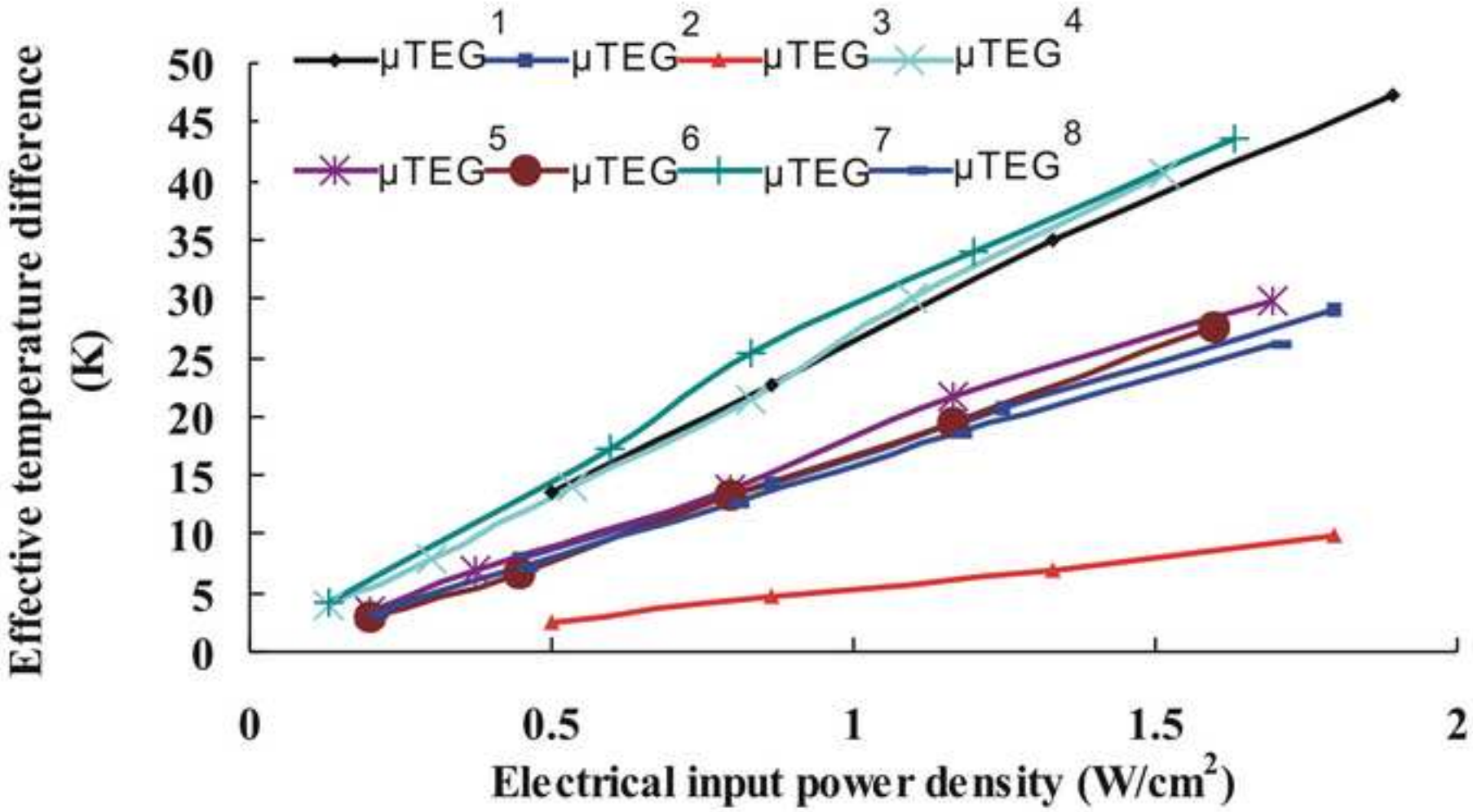
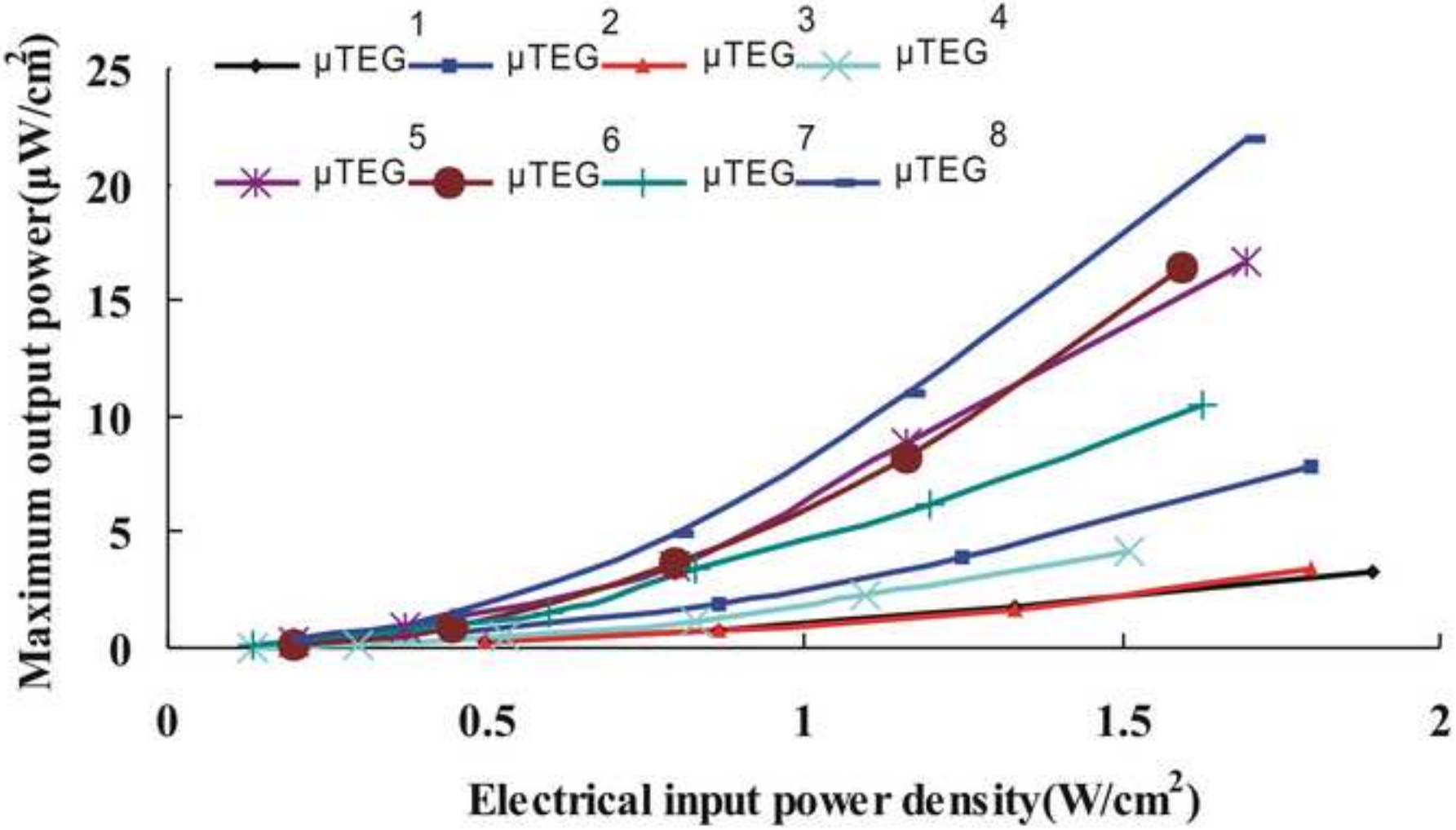

μTEG1
μTEG2
μTEG3
μTEG4
μTEG5
μTEG6
μTEG7
μTEG8
Effective temperature difference (K)
50
45
40
35
30
25
20
15
10
5
0
0
0.5
1
1.5
2
Electrical input power density (W/cm2)

Figure13


μTEG1
μTEG2
μTEG3
μTEG4
μTEG5
μTEG6
μTEG7
μTEG8
Maximum output power(μW/cm2)
25
20
15
10
5
0
0
0.5
1
1.5
2
Electrical input power density(W/cm2)